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32X
Hardware Manual
Supplement 1

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Pg. 67 Communication

1. About the 3ZX System Register

The 3ZX system register can cause a mistake in reading if simultaneously performing read and write from the 68000 and SH2. However, except for the communication and PWM registers, since there are many registers that can not access from both 68000 and SH2, or from 68000 to SH2, even when reading and writing at the same time, the read side will continue reading two times, and it will be determined that correct data is being read when they coincide.

Development boards until the Target ver 3.1, and the ver 3.2 development board already shipped, could simultaneously read and write from both directions, but not the revision of development boards and devices since then. This is because the design that originally allowed read and write bidirectionally had to be functionally cut due to the chip size. As a result, be aware that the development board and device may not operate even by the program currently operating.

On the following page is an example of a communication register in which read and write are frequently done at the same time. A problem to be aware of with simultaneous read/write are system registers that can satisfy read and write from other opposite directions, and not necessarily the communication register. The 3ZX has 8-word communication registers which are able to write in byte and word units, however, when accessing the same address please note the following points.

1) The same address cannot read simultaneously from both SH2 and 68000.

2) When writing the same address simultaneously from both SH2 and 68000, one of the values is written, but which one can not be predicted since it is controlled by write timing. However, there is no problem in accessing the same address simultaneously when divided by byte units; one direction is significant at 8-bit and the other direction insignificant 8-bit.

3) When simultaneously reading, on the one hand, and writing, on the other hand, the same byte or words of the same address from both the SH2 and the 68000, the write process will definitely occur but mistakes may occur in the read process. That is due to the fact that the time in which data written on one side is transferred to the other side within the LSI chip differs according to the bit. But there is no problem in accessing the same address simultaneously when divided by byte units, one direction significant 8-bit and the other direction insignificant 8-bit.

Example

Assume the 68000 uses communication register A1$1201 and transports instructions to SH2. SH2 always reads 4020H and performs various operations from values written by commands. Once the proper type of commands are written in FFFFH, AAAAH, and 5555H SH2 restarts commands, then by writing 0680H when the operation ends, lets the 68000 know all the instructions are done, and waits. The 68000 constantly monitors this area between FFFFH and 5H in simultaneously reading, SH2 can read which ever value of 0680H ... FFFEH, AAAAEH or 7FFFH commands are being started. So overall then, if the 68000 reads real values directly at both sides in the communication register requires data already [ ] list mode [ ] send. In other words: one bit can only have one meaning. If with constant ... bit this data is already written and the data that is to be written next, the set up does not allow a single to change; then errors could occur in the example.

d) Measuring can be invaded by using a data format bus [bit in 1 word such as instruction commands 0305H, 0350H, and 3501H. But in this case only 16 types of commands can be transferred.

b) Command written to A1$1201, and A1$0201 gives a flag that shows simple command write. After a command is written to A1$201 68000 writes 0620 to A1$1201. SH2 writes 1000 to 4020H when the operation ends.

2. Actual FIFO

The configuration of FIFO is 4 words X 2 of block A FIFO and block B FIFO. Figure 1 shows the actual configuration. (The original configuration differs considerably, but this configuration should be thought of as a type). The operations explained next When FIFO is used, latch DREQ by active H 1st edge, set the dual address model and transfer destination to 6012H, then put the buffer transfer size in word unit. DACK is not used with the 3/F chip, therefore are writing at all eight, 1/F0 should be used in 4-word units. The 68000, after each word of data on the DREQ relationship has been set, sets the DREQ control against in response to the transfer type.

The 68000 directly writes to H1C into /b13-2H the data that you want to be transferred to SH2. FIFO blocks writings to first because it is the 1st asserted. Because all of FIFO block is fixed in case of the 4 words are written, the write destination is switched to FIFO block B. After which, a FIFO block is switched each time a 4 block is filled. When a block A FIFO block is switched back each block when word words are written, the 68000 should write the next 4 words after confirming whether A1$056H, bit 7 of the DREQ control register, and FIFO full bit on 0 An operation in which mode is written while FIFO is full becomes undefined. The 1/F chip sets DREQ0 to SH2 to H and activates DMA, at the start that 1 FIFO block and 4 words are full, SH2 should read 1/F0 block and DREQ output of the 1/F0 chip becomes L. After this, DREQ 0 becomes H each time a FIFO block, inferring a minimum 4 items in the direction, is empty. When a DMA transfers end, the SH2 read FIFO block switches ... DREQ 0 becomes H when all the switched FIFO blocks are written. by the 68000, and the DMA transfer request is

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sent again as previously mentioned. The operation on the previous page is then repeated until DMA transfer is done, the number of times that the length is written to A1513H and 48 to SH DREQ Length. FIFO Full occurs when 6600 selects the block that SH2 is sending or is going to read to the write destination. When all transfer of the 6600 side has ended, 685 of bit 2 of A1520H automatically becomes 0 and FIFO access of the 6600 side ends. Then 6600H (system anything written to A1512H and FIFO DMA transfer requests are sent by DREQ 0 and all DMA transfer for SH2 have ended. Thus, the communication request should be used when SH2 side request end must be reported from the SH2 side to 6600 since it is not known whether or not DMA transfer of the SH2 side has ended, even 685 is 0. If 685 becomes 0 while 6600 is transferring, DMA transfer can be forcefully interrupted, but because the SH2 side doesn't report the end of DMA transfer during that time, forces DREQ 0 to become L operation after that is undefined. The value of the counter that indicates the write destination on FIFO itself is also undefined. Thus, only when SH systems such as VBLERT are reset or when a SH2 side operation is controlled by 6600 should you use DMA forced read/reg writing 0 to 685. On the other hand, when a system has been reset, 685 (structure of the transfer in progress can be performed and you should, therefore, write 0 to 685.
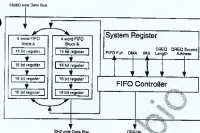
Fig. 1 Configuration of a More a more

3. About VDP Access

The 32X VDP is done through the VDP1/F circuit of the I/F Bridge to the VDP chip VDP variation across of the 68000 and SH2 simply by A31[69]/A6008 for SH2) of the 15 and the FM bit. Appears more a micro diagram of the SH2, 68000, I/F chip and VDP chip. The SH2 side base 2 areas write cycle for the frame buffer and can actually wrap up to a continuous 16 cycles by 3 times passing in the minimum cycle during the external space of SH2. Reading to other VDP registers, palette, and all VDP requires at least 2 clocks. When reading to the VDP pertaining to the VDP register and palette immediately after writing to the frame buffer, after all the data currently in the cache is transferred to the VDP side, composed in manual independent access, a large number of reads are entered against the SH2, thus prolonging the access time.

One point of caution is when, in the worst case scenario, transfer to the VDP becomes obstructed and SH2, 68000, as well as the VDP, lock up because access authentication is forced to the 68000 side of the I/F circuit is writing to the frame buffer VDP if the FM bit is set to 0 immediately after SH2 finishes writing to the frame buffer. Accordingly, when switching the FM bit, it must be done after reading to the frame buffer, VDP register or palette (or writing to the VDP register and palette) and all cache data is transferred to the VDP.
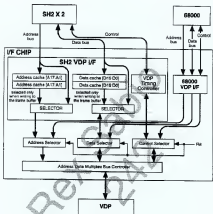
Fig. 2 Block Diagram of SH2, 68000, I/F Chip and VDP Chip